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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,863	09/06/2006	Simon Dcleonibus	129344	3443

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EXAMINER	
KUO, WENSING W	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
11/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,863	DELEONIBUS, SIMON	
	Examiner	Art Unit	
	W. Wendy Kuo	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06 September 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear whether Applicant is claiming an NMOS type transistor, a PMOS type transistor, or both.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Orlowski et al. (US 2006/0043498) (hereinafter Orlowski).

5. Orlowski (e.g. Figure 7) teaches a field effect transistor comprising a source 23, a drain 33, and a channel 18, respectively formed by source, drain, and channel materials, the source, drain, and channel materials selected such that

- For a NMOS type transistor, the electronic affinity of the drain material (SiC) is lower than the electronic affinity of the channel material (Si) [0028], and such that
- For a PMOS type transistor, the upper level of the valence band of the drain material (SiGe) is higher than the upper level of the valence band of the channel material (Figure 8),

The transistor being of the normally on type,

- The electronic affinity of the source material of NMOS transistor is higher than the electronic affinity of the channel material of said NMOS transistor [0024], and
- The upper level of the valence band of the source material of a PMOS transistor is lower than the upper level of the valence band of the channel material of said PMOS transistor (Figure 8).

*Note that the materials disclosed by Orlowski (e.g. silicon, silicon carbide, silicon germanium) inherently have the relational electronic affinity/valence band properties as claimed by Applicant. Please see Forbes (US 5,801,401) (column 4, lines 10-13) for electron affinity values of silicon and silicon carbide.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Orlowski as applied to claim 1 above in view of Ohata (US 4,556,895) (hereinafter Ohata).

8. Orlowski fails to teach an integrated circuit comprising PMOS type and NMOS type field effect transistors according to claim 1. Ohata teaches that it is advantageous to fabricate an IC with complementary transistors in order to reduce power consumption (column 1, lines 19-21).

It would have been obvious to one of ordinary skill in the art at the time of the invention to fabricate a PMOS type and NMOS type field effect transistor as taught by Orlowski in an integrated circuit as taught by Ohata for the benefit of reducing power consumption.

9. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester (US 5,166,084) (hereinafter Pfiester) in view of Currie et al. (US 5,986,291) (hereinafter Currie), and further in view of Valone (US 5,602,439) (hereinafter Valone).

10. With respect to claim 1, Pfiester (e.g. Figure 4) teaches a field effect transistor comprising a source 18, a drain 18, and a channel 16, respectively formed by source, drain, and channel materials (column 3, lines 40-46), the drain and channel materials being selected such that

- For a NMOS type transistor, the electronic affinity of the drain material (GeSi) is lower than the electronic affinity of the channel material (Si),
- For a PMOS type transistor, the upper level of the valence band of the drain material is higher than the upper level of the valence band of the channel material.

*Note that the drain and channel materials as disclosed by Pfiester (e.g. germanium silicon and silicon) inherently have the relational electronic affinity/valence band properties as claimed by Applicant.

Pfiester fails to teach that for the transistor being of the normally on type

- The electronic affinity of the source material of NMOS transistor is higher than the electronic affinity of the channel material of said NMOS transistor and
- The upper level of the valence band of the source material of a PMOS transistor is lower than the upper level of the valence band of the channel material of said PMOS transistor.

Currie teaches that it is beneficial to provide a FET device with a source region having a low electron affinity near the channel region in order to accelerate charge carriers and increase switching speed (column 4, lines 9-13 and lines 46-52). Valone teaches that diamond-like carbon is a material having low electron affinity (column 4, lines 12-24) that is beneficial to use in order to provide a field emitter having high electron emission efficiency (column 2, lines 17-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the field effect transistor of Pfiester with the low electron affinity diamond-like carbon source region as taught by Currie and Valone for the benefit of increasing switching speeds and providing high electron emission efficiency.

*Note that the respective materials taught by Pfeister as modified by Currie and Valone (e.g. germanium silicon, silicon, diamond-like carbon) for the drain, channel, and

source inherently have the relational electronic affinity/valence band properties as claimed by Applicant.

11. With respect to claim 2, Pfeister further teaches an integrated circuit comprising PMOS and NMOS type field effect transistors according to claim 1 (column 1, lines 34-39).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. Wendy Kuo whose telephone number is (571) 270-1859. The examiner can normally be reached Monday through Friday 7:00 AM to 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached at (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Wendy Kuo

W. Wendy Kuo
Examiner
Art Unit 2826

WWK

LEONARDO ANDUJAR
PRIMARY EXAMINER